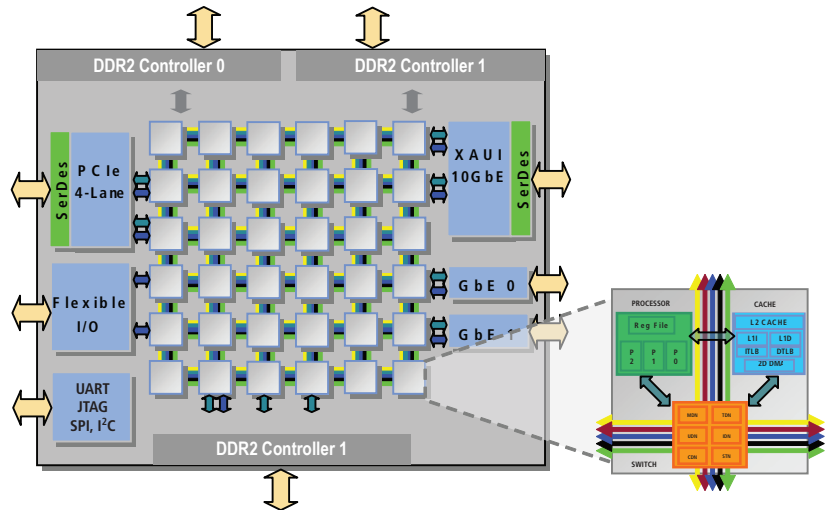


### Overview

The TILEPro36™ processor brings the power of multicore computing to the mid range of the embedded market. This revolutionary processor features 36 identical processor cores (tiles) interconnected with Tileras iMesh™ on-chip network. Each tile is a complete full-featured processor, including integrated L1 and L2 cache and a non-blocking switch that connects the tiles into the iMesh network. As with all Tileras processors, each tile can independently run a full operating system, or a group of multiple tiles can run a multi-processing OS like SMP Linux.

The TILEPro™ family incorporates numerous Tileras innovations such as DDC™ (Dynamic Distributed Cache) that accelerates coherent cache performance by a factor of two compared with other multicore designs. Further, the TileDirect™ technology provides coherent I/O directly into the tile caches to deliver ultimate low-latency packet processing performance.



By integrating a complete set of memory and I/O controllers, the TILEPro36 eliminates the need for an external north bridge or south bridge – slashing board real estate requirements and system costs. The high-speed flexible I/O subsystem provides a configurable interface to peripheral devices, such as video cameras, displays, or bitstream feeds.

The TILEPro36 processor is programmed in ANSI standard C and C++, enabling developers to leverage their existing software investment. Tiles can be grouped in clusters to apply the appropriate amount of horsepower to each application. Since multiple operating system instances can be run on the TILEPro36 simultaneously, it can replace multiple CPU subsystems for both the data plane and control plane.

The TILEPro36 processor is socket and software compatible with the TILE64™ and TILEPro64™.

	Features	Enables
Massively Scalable Performance	<ul style="list-style-type: none"> <li>6 X 6 grid of general-purpose processor cores (tiles)</li> <li>32-bit VLIW processors using a 64-bit instruction bundle</li> <li>3-deep pipeline with up to 3 instructions per cycle</li> <li>2.8 Mbytes of on-chip cache</li> <li>Up to 144 billion operations per second (32-bit)</li> <li>12 Tbps of on-chip mesh interconnect</li> </ul>	<ul style="list-style-type: none"> <li>5 Gbps Snort® processing</li> <li>5 Gbps iptables (firewall)</li> <li>X.264 HD encode for 2 streams of 720p30 (main profile)</li> <li>5 channels of OFDM wireless baseband processing</li> </ul>
Power Efficiency	<ul style="list-style-type: none"> <li>9-13 Watts for typical applications</li> <li>500MHz operating frequency</li> <li>Idle Tiles can be put into low-power sleep mode</li> <li>Power efficient inter-tile communications</li> </ul>	<ul style="list-style-type: none"> <li>Highest performance per watt</li> <li>Simple thermal management and power supply design</li> <li>Small system form factor</li> <li>High-speed I/O to peripherals such as HDD, USB, etc.</li> </ul>
Integrated Solution	<ul style="list-style-type: none"> <li>Three, 64-bit DDR2 memory controllers with optional ECC</li> <li>10Gbps Ethernet XAUI packet interface</li> <li>4-lane PCIe interface; root complex or endpoint mode</li> <li>Two GbE MAC interfaces</li> <li>64-bit Flexible I/O interface, with four independent clock domain</li> </ul>	<ul style="list-style-type: none"> <li>Reduces BOM costs by making standard interfaces on-chip</li> <li>Dramatically reduced board real estate</li> <li>Direct interface to leading L2-L3 switch vendors</li> </ul>
Multicore Development Environment Options	<ul style="list-style-type: none"> <li>ANSI standard C/C++ compiler</li> <li>Advanced profiling and debugging designed for multicore programming</li> <li>Supports SMP Linux with 2.6 kernel</li> <li>Multicore communication APIs for efficient inter-tile data transfer</li> </ul>	<ul style="list-style-type: none"> <li>Running off-the-shelf C/C++ programs</li> <li>Reduction of debug and optimization time</li> <li>Faster time to production code</li> <li>Standard multicore communication mechanisms</li> </ul>

# TILEPro36 Processor – Product Brief

## Processing Flexibility

The processor core in the TILEPro36 combines the features of a general-purpose CPU together with powerful signal processing and SIMD capabilities. As a result, it can integrate multiple functions on a single processor, reducing system cost and simplifying system design. For example, it can transcode multiple streams of video and perform audio echo cancelling while simultaneously running encryption and network stack functions. A robust protection-level hierarchy with virtual memory and Tiler's Multicore Hardwall™ technology provide kernel-level protection related to both shared memory and user-level streaming and messaging.

## Target Applications

The TILEPro36 processor has both the flexibility and performance to support a wide range of computing-intensive applications, including advanced networking, digital multimedia, telecommunication and wireless infrastructure.

## Intelligent Networking Products

The TILEPro36 processor is ideally suited for 2-5 Gbps intelligent network services including:

- Intrusion detection/prevention (IDS/IPS)
- Unified Threat Management (UTM)
- L4-7 Deep Packet Inspection
- Network monitoring and forensics
- Quality of Service (QoS) provisioning

## Digital Multimedia Products

The TILEPro36 processor also excels at digital audio and video processing, taking the place of multiple DSPs or FPGAs and a control processor:

- Video transcoding/transrating
- Professional video editing and encoding
- Streaming IPTV and video on demand (VoD)
- Ad insertion
- Video post-production processing

## Wireless Infrastructure

In current GSM/CDMA and next generation WiMAX and LTE wireless networks, the TILEPro36 provides a unified, programmable computing solution for:

- Base transceiver station (BTS)
- Base station controller (BSC)
- Wireless backbone gateways (GGSN, SGSN, media gateway)

## Ordering Information

Part Number	I/O Interfaces	Processor Frequency	DDR2 Memory Speed	Number of Tiles	Package	Operating Temperature
TLR3-36040BG-5C	1 PCIe, 1XAUI, 2 GbE, and 64-bit Flexible I/O	500 MHz	3 @ 533MHz	36	1517 BGA	0-70 °

## Development Environment

Tiler's Multicore Development Environment™ (MDE) is a complete standards-based multicore programming solution that enables developers to take full advantage of the parallel processing potential of the Tile Processor™ architecture.

Powerful innovations allow the developer to take a Gentle Slope Programming approach to multicore software development. By leveraging Open Source software and the developer's existing software codebase, impressive results can be achieved in an extremely short period of time. As developers become more familiar with large-scale multicore, they can take advantage of the enhanced tools and libraries offered in the MDE.

Tiler's MDE includes:

- Standard Eclipse-based IDE
- ANSI C/C++ compiler
- Multi-tile timing-accurate simulator
- Whole chip debug and performance analysis
- Complete SMP Linux support
- Multicore communication APIs for efficient inter-tile data transfer
- PCI Express hardware development platform
- Linux host environments

## Scalable Processing and Ease of Use for Embedded Application Developers

The TILEPro36 addresses developers' needs for scalable multiprocessor performance, with the highest performance per watt and ease of programming. The TILEPro family specifically accelerates threaded and shared-memory applications, giving unprecedented results with unmodified code.

With the on-chip iMesh network, DDC architecture, and the industry's best multicore development tools, Tiler provides solutions that are uniquely suited to today's networking, multimedia, and wireless applications.