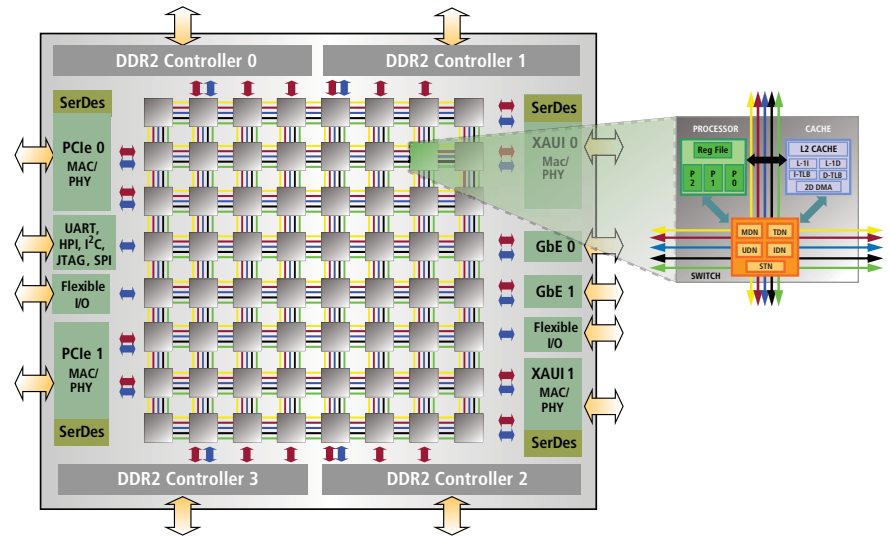


Overview

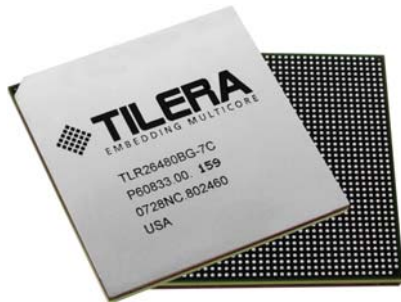
The TILE64™ family of multicore processors delivers immense computing performance to drive the latest generation of embedded applications. This revolutionary processor features 64 identical processor cores (tiles) interconnected with Tiler's iMesh™ on-chip network. Each tile is a complete full-featured processor, including integrated L1 and L2 cache and a non-blocking switch that connects the tile into the mesh. Each tile can independently run a full operating system, or a group of multiple tiles can run a multi-processing OS like SMP Linux.



The TILE64 processor family slashes board real estate and system costs by integrating a complete set of memory and I/O controllers, therefore eliminating the need for an external North Bridge or South Bridge. Tiler's architectural innovations deliver scalable performance, power efficiency and low processing latency in an extremely compact footprint.

The TILE64 Processor is programmable in ANSI standard C and C++, enabling developers to leverage their existing software and maximize their investments. Tiles can be grouped into clusters to apply the appropriate amount of horsepower to each application. Since multiple operating system instances can be run on the TILE64 simultaneously, it can replace multiple CPU subsystems for both the data plane and control plane.

Combining multiple C-programmable processor tiles with the iMesh multicore technology enables the TILE64 processor to achieve the performance of a fixed function ASIC or FPGA in a powerful software-programmable solution.


Product Differentiators

	Features	Enables
Massively Scalable Performance	<ul style="list-style-type: none"> 8 X 8 grid of identical, general purpose processor cores (tiles) Three-way VLIW pipeline for instruction level parallelism 5 Mbytes of on-chip cache Up to 443 billion operations per second (BOPS) 31 Tbps of on-chip mesh interconnect enables linear application scaling Up to 50 Gbps of I/O bandwidth 	<ul style="list-style-type: none"> 10 Gbps Snort® processing 20 Gbps nProbe 16 X 16 SAD at 540 MBlocks/s H.264 HD video encode: 2+ streams of 720p30
Power Efficiency	<ul style="list-style-type: none"> 700MHz - 866MHz operating frequency 15 - 22W @ 700MHz all cores running full application Idle Tiles can be put into low-power sleep mode Power efficient inter-tile communications 	<ul style="list-style-type: none"> Highest performance per watt Simple thermal management and power supply design Lower operating cost
Integrated Solution	<ul style="list-style-type: none"> Four DDR2 memory controllers with optional ECC Two 10GbE XAUI configurable MAC or PHY interfaces Two 4-lane PCIe interfaces: Root complex or endpoint mode Two GbE MAC interfaces Flexible I/O interface 	<ul style="list-style-type: none"> Reduces BOM cost – standard interfaces included on-chip Dramatically reduced board real estate Direct interface to leading L2-L3 switch vendors
Multicore Development Environment	<ul style="list-style-type: none"> ANSI standard C / C++ compiler Advanced profiling and debugging designed for multicore programming Supports SMP Linux with 2.6 kernel Tiler Multicore Components (TMC™) libraries for efficient inter-tile communication 	<ul style="list-style-type: none"> Run off-the-shelf C programs Reduce debug and optimization time Faster time to production code Standard multicore communication mechanisms

TILE64™ Processor – Product Brief

Targeted Applications

The TILE64 family of processors has both the flexibility and performance to support a wide range of computing-intensive applications, including advanced networking, digital video, and telecommunication. Because it is a general-purpose MIMD multicore processor, it can run multiple operating systems and applications simultaneously. For example, it can perform 10Gbps of TCP offload (TOE) along with multiple streams of video transcoding. Virtual memory support and Tiler's Multicore Hardwall™ technology provides kernel-level protection related to both shared memory and user-level streaming and messaging.

Advanced Networking Products. The TILE64 processor is ideally suited to intelligent network services such as Unified Threat Management (UTM), L4-7 Deep Packet Inspection, or Quality of Service (QoS) provisioning. The impressive computing performance together with a complete integrated networking I/O subsystem makes the TILE64 a powerful single-chip communications processor.

Digital Multimedia Products. The TILE64 processor also excels at digital video and audio processing, easily taking the place of multiple DSPs to perform audio/video encoding, transcoding, video analytics, or other digital video manipulation. In addition, the control plane and any required networking capability can be handled by the same TILE64 device.

Since this processor is available in multiple power/performance configurations, the family can address varying price and performance needs.

Development Environment

Tiler's Multicore Development Environment™ (MDE) is a complete standards-based multicore programming solution that enables developers to take full advantage of the parallel processing potential of the Tile Processor™ architecture.

Powerful innovations allow the developer to take a Gentle Slope Programming™ approach to multicore software development. By leveraging Open Source software and the developer's existing software code base, designers can achieve impressive results in an extremely short period of time. Then, as developers become more familiar with large-scale multicore processing, they can take advantage of the enhanced tools and libraries offered in the MDE to optimize performance further.

Tiler's MDE includes:

- Standard Eclipse-based IDE
- ANSI standard C / C++ compiler
- Multi-tile cycle-accurate simulator
- Whole chip debug and performance analysis
- Complete SMP Linux support
- TMC library for efficient inter-communication
- PCIe Hardware development platform
- Linux and Windows host environments

Scalable Processing and Ease of Use for Embedded Application Developers

The TILE64 Processor addresses application developers' needs for scalable multiprocessor performance, performance per watt, and ease of development. The Tile Processor's on-chip iMesh network, the distributed cache architecture, and the industry-standard development tools combine to provide a solution uniquely suited to today's networking and multimedia applications.

Ordering Information

Part Number	Description	I/O Interfaces	Processor Frequency	DDR2 Memory Speed	Number of Tiles	Package	Operating Temperature
TLR26480-BG-7C	Standard	2 XAUI, 2 PCIe, 2 GbE	700MHz	800MHz	64	1517 BGA	0-70° Commercial
TLR26480-BG-9C	High-Performance	2 XAUI, 2 PCIe, 2 GbE	866MHz	800MHz	64	1517 BGA	0-70° Commercial

For more information on Tiler products, visit www.tiler.com.

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